AMENDMENTS TO THE CLAIMS

Claims 1-75 (Canceled)

Claim 76 (Previously Presented) An integrated circuit, comprising:

a first function block having a plurality of inputs and a plurality of outputs;

a first channel coupled to a first portion of the plurality of inputs located on a first side of the first function block and coupled to a first portion of the plurality of outputs located on the first side of the first function block;

a second channel coupled to a second portion of the plurality of inputs located on a second side of the first function block, the second side opposite the first side, and coupled to a second portion of the plurality of outputs located on the second side of the first function block;

a third channel coupled to the first channel and the second channel and coupled to a third portion of the plurality of inputs located on a third side of the first function block and coupled to a third portion of the plurality of outputs located on the third side of the first function block; and

a fourth channel associated with a fourth side of the function block that is opposite the third side, the fourth channel coupled only to the first channel and the second channel.

Claim 77 (Previously Presented) The integrated circuit of claim 76, wherein there is a difference between any two of: (a) a number of a first plurality of wires within the first channel, (b) a number of a second plurality of wires within the second channel, or (c) a number of a third plurality of wires within the third channel.

Claim 78 (Previously Presented) The integrated circuit of claim 76, further comprising:

a wire driving device having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to a particular one of the plurality of outputs on a particular function block side that is any one of the first side, the second side, or the third side of the first function block, the wire driving device driving a signal, output by the first function block, on a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second

channel, or a third plurality of wires within the third channel that is associated with the particular function block side; and

an input multiplexer having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the first plurality of wires within the first channel, the second plurality of wires within the second channel, or the third plurality of wires within the third channel that is associated with the particular function block side,

wherein the wire driving device is upstream from the input multiplexer.

Claim 79 (Previously Presented) The integrated circuit of claim 78, wherein the wire driving device drives the signal to at least one of the particular one of the plurality of inputs of the input multiplexer, and up to a length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires minus a length of the first function block away.

Claim 80 (Previously Presented) The integrated circuit of claim 76, further comprising:

an input multiplexer having a plurality of inputs and an output, the output coupled to a particular one of the plurality of inputs on a particular function block side that is any one of the first side, the second side, or the third side of the first function block; and

a wire driving device having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to a particular one of the plurality of outputs on the particular function block side, the output of the wire driving device driving a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the particular function block side,

wherein the input multiplexer is upstream from the wire driving device.

Claim 81 (Previously Presented) The integrated circuit of claim 80, wherein the wire driving device drives a signal up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires away.

Claim 82 (Previously Presented) The integrated circuit of claim 76, further comprising:

a second function block having a plurality of inputs and a plurality of outputs;

an input multiplexer having a plurality of inputs and an output, the output coupled to a particular one of the plurality of inputs of the first function block; and

a wire driving device having a plurality of inputs and an output, a first one of the plurality of inputs of the wire driving device coupled to a particular one of the plurality of outputs of the first function block, and a second one of the plurality of inputs of the wire driving device coupled to a particular one of the plurality of outputs of the second function block, and the output of the wire driving device coupled to a particular one of the plurality of inputs of the input multiplexer,

wherein the wire driving device is downstream from the second function block and the wire driving device is upstream from the input multiplexer and the first function block.

Claim 83 (Previously Presented) The integrated circuit of claim 82, wherein the output of the wire driving device is coupled to a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the wire driving device.

Claim 84 (Previously Presented) The integrated circuit of claim 83, wherein the wire driving device drives a first signal from the second function block up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires away, or the wire driving device drives a second signal from the first function block to at least one of: (a) the particular one of the plurality of inputs of the input multiplexer, and (b) up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires minus the length of the first function block away.

Claim 85 (Previously Presented) The integrated circuit of claim 76, wherein a particular one of the plurality of inputs or a particular one of the plurality of outputs of the first function block is coupled to at least two of the first channel, the second channel, or the third channel.

Claim 86 (Previously Presented) The integrated circuit of claim 85, wherein the coupling to the third channel is coupling to a particular one of a third plurality of wires within the third channel, the coupling to the first channel is coupling to a particular one of a first plurality of wires within the first channel, and the coupling to the second channel is coupling to a particular one of a second plurality of wires within the second channel.

Claim 87 (Previously Presented) The integrated circuit of claim 76, wherein a particular one of the plurality of outputs of the first function block is directly coupled to a particular one of a plurality of inputs of a second function block.

Claim 88 (Previously Presented) The integrated circuit of claim 87, further comprising: an input multiplexer, coupled to the second function block and having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the plurality of outputs of the first function block and the output of the input multiplexer coupled to the particular one of the plurality of inputs of the second function block.

Claim 89 (Previously Presented) The integrated circuit of claim 76, wherein the integrated circuit is a programmable logic device.

Claim 90 (Previously Presented) The integrated circuit of claim 76, wherein the first function blocks is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

Claim 91 (Previously Presented) A digital system including the integrated circuit of claim 76.

Claim 92 (Previously Presented) An electronic system, comprising:

a processor that includes a programmable logic device as in claim 76;

a memory to store information;

an interface; and

a bus to couple together the processor, the memory, and the interface.

Claim 93 (Previously Presented) The electronic system of claim 92, wherein the processor configures the programmable logic device.

Claim 94 (Currently Amended) A method to interconnect a function block within a programmable logic array, comprising:

transmitting and receiving signals between a first portion of a plurality of pins on a first side of the function block and a first channel;

transmitting and receiving signals between a second portion of the plurality of pins on a second side of the function block and a second channel, the second side opposite the first side;

transmitting and receiving signals between a third portion of the plurality of pins on a third side of the function block and a third channel; and

~~preventing transmission and receipt of signals between the function block and~~ transmitting and receiving signals between a fourth channel associated with a fourth side of the function block and only the first channel and the second channel, the fourth side opposite the third side.

Claim 95 (Previously Presented) The method of claim 94, further comprising:

differing any two of: (a) a number of a first plurality of wires within the first channel, (b) a number of a second plurality of wires within the second channel, or (c) a number of a third plurality of wires within the third channel.

Claim 96 (Previously Presented) The method of claim 94, further comprising:

at least one of: (a) driving a signal on a particular one of a plurality of wires within the first channel, the second channel, or the third channel up to a length of the particular one of the plurality of wires minus a length of the function block away, and receiving the signal on the particular one of the plurality of wires.

Claim 97 (Previously Presented) The method of claim 94, further comprising:

driving a signal on a particular one of a plurality of wires within the first channel, the second channel, or the third channel up to the length of the particular one of the plurality of wires away.

Claim 98 (Previously Presented) The method of claim 94, further comprising:

at least one of: (a) driving a first signal, transmitted by the function block, on a particular one of a plurality of wires within the first channel, the second channel, or the third channel up to the length of the particular one of the plurality of wires minus the length of the function block away, (b) driving a second signal, transmitted by another function block, on the particular one of the plurality of wires up to the length of the particular one of the plurality of wires away, and (c) receiving, by the function block, the first signal or the second signal on the particular one of the plurality of wires.

Claim 99 (Previously Presented) The method of claim 94, further comprising:

coupling a particular one of the plurality of pins of the function block to the third channel and at least one of the first channel and the second channel.

Claim 100 (Previously Presented) The method of claim 94, further comprising: directly coupling a particular one of the plurality of pins of the function block to a particular one of a plurality of pins of another function block.